

High Precision Large Core Fiber Variable Attenuator

(0.2-2mm fiber core size, high setting precision, little drift)



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The HPLA Series VOA is based on moving fiber technology with a precision motor featuring low optical loss. This broad spectral band is only limited by fiber intrinsic properties and precision/repeatability for fibers with large core sizes up to 2mm in diameter. It is designed for high precision and high fidelity measurements with little optical mode dependence. Conventional light deflections and blockings affect light transmission characteristics, but fiber-fiber technology overcomes this by eliminating coating and Lens. The HPLA has two built-in optical position sensors so that once the VOA attenuation value is set, it will remain at the value regardless of the environment variations. It has a high repeatability of 0.1dB and a high resolution. Once powered, it is a latching device that can be operated in vibration environments.

The VOA integrates with a USB or RS232 driving PCB with GUI. A wall pluggable power supply is provided.

Features

- Low Loss
- 0.1dB Repeatable
- 70dB Attenuation
- SM, PM, MM
- USB

Applications

- Power Control
- Measurement
- Calibration
- Instrumentation

Specifications

Parameter	Min	Typical	Max	Unit
Wavelength Center	300		2400	nm
Insertion Loss [1]	0.4	0.6	1.2	dB
Polarization Dependent Loss [2]		0.15	0.5	dB
Wavelength Dependence Loss [2]		0.1	0.2	dB
Attenuation Range	50	60	80	dB
Attenuation Resolution (10bit step motor)		0.1		dB
Accuracy/Repeatability	0.6-30dB 30-60dB	0.5	1	dB
Return Loss	45			dB
Response (step)	50		500	ms
Power Consumption			1	W
Optical Power handling (CW)		500	800	mW
Operating Temperature	-5		60	°C
Storage Temperature	-40		85	°C

Notes:

[1]. Without connector and at room temperature

[2]. At attenuation less than 20 dB

Note: The specifications provided are for general applications with a cost-effective approach. If you need to narrow or expand the tolerance, coverage, limit, or qualifications, please [click this link](#):

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Electrical Control Interface

The VOA can be controlled by a computer via a USB interface. It uses a Micro USB type B connector that also provide power to the VOA at the same time. The device accept UART command and recognized as a serial device by the PC.

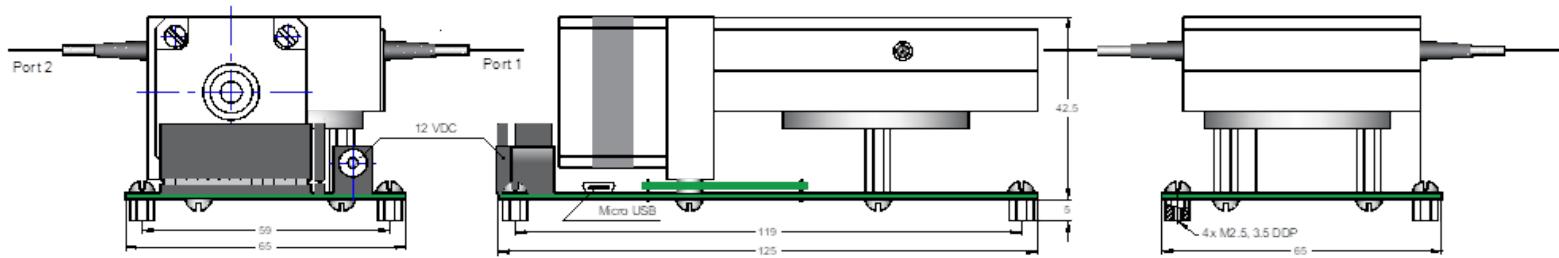
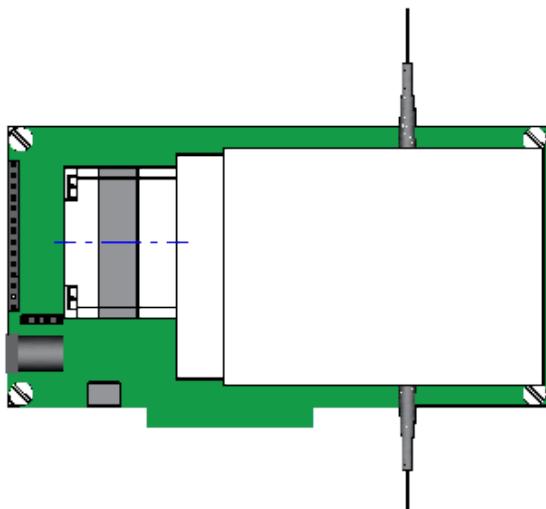
Pin 1 – 0V

Pin 2 – 5V DC Power

Pin 4 – 0V

Pin 5 – 0-5V Control

Mechanical Footprint Dimensions (mm)



*Product dimensions may change without notice. This is sometimes required for non-standard specifications.

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Typical Stability

Typical Control Response

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Typical Optical Rise/Fall Time

Typical Insertion Loss vs Wavelength (1240-1630nm)

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Ordering Information

	1	<input type="checkbox"/>	1	<input type="checkbox"/>	1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Prefix	Type	Controller	Test Wavelength			Fiber Type	Fiber Cover	Fiber Length	Connector		
HPLA-	Standard = 1 Special = 0	USB = 1 RS232 = 2		1240-1620 = 1 1310 = 3 1550 = 5 850 = 8 Special = 0		105/NA.22 = E 200/NA.22 = F 300/NA.22 = G 400/NA.22 = H 600/NA.22 = J 800/NA.22 = K Special = 0	900um tube = 3 2 mm Jacket = 2 Special = 0	0.25m = 1 0.5m = 2 1.0m = 3 Special = 0	None = 1 FC/PC = 2 SC/PC = 4 SMA = 8 Special = 0		

Application Notes

Fiber Core Alignment

Note that the minimum attenuation for these devices depends on excellent core-to-core alignment when the connectors are mated. This is crucial for shorter wavelengths with smaller fiber core diameters that can increase the loss of many decibels above the specification if they are not perfectly aligned. Different vendors' connectors may not mate well with each other, especially for angled APC.

Fiber Cleanliness

Fibers with smaller core diameters (<5 µm) must be kept extremely clean, contamination at fiber-fiber interfaces, combined with the high optical power density, can lead to significant optical damage. This type of damage usually requires re-polishing or replacement of the connector.

Maximum Optical Input Power

Due to their small fiber core diameters for short wavelength and high photon energies, the damage thresholds for device is substantially reduced than the common 1550nm fiber. To avoid damage to the exposed fiber end faces and internal components, the optical input power should never exceed 20 mW for wavelengths shorter 650nm. We produce a special version to increase the handling by expanding the core side at the fiber ends.

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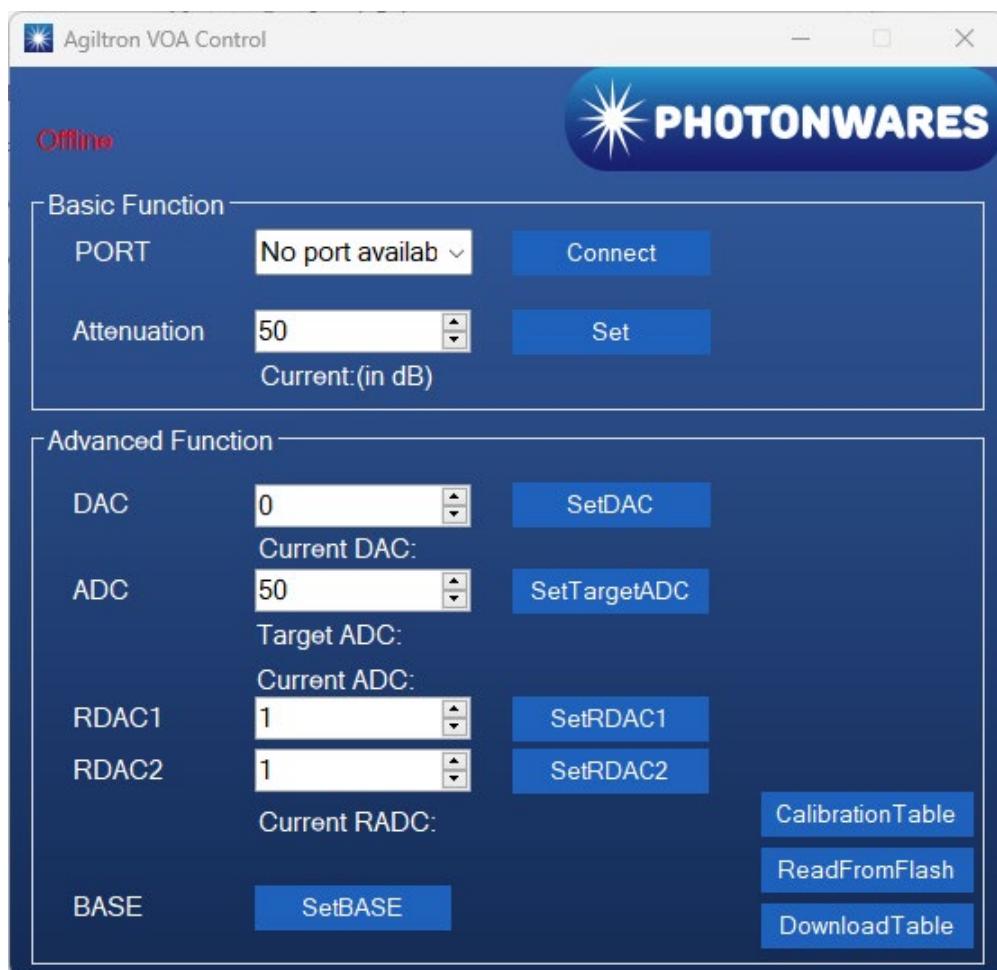


Figure 1. Test GUI

Control via Windows GUI:

Basic:

1. Connect device

PORT

Choose the correct COM port, then click "Connect" button to connect with the device.

2. Set target DB for VOA

Attenuation
Current:(in dB) 3000

Type the DB value in the number box, then click "Set" button to set target DB value. The current DB value would change to the set value if successful.

DB value 1000 means -10.00 DB attenuation.

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Control via Windows GUI:

Advanced

3. Control Piezo VOA via DAC (Directly set voltage)

DAC	<input type="text" value="0"/>	<input type="button" value="SetDAC"/>
Current DAC: 2562		

Type the value of DAC in the number box, then click “Set” button to set the value. The value should be between 0 and 4000.

4. Control Piezo VOA via ADC (Feedback control, maintain the ADC to a certain value)

ADC	<input type="text" value="50"/>	<input type="button" value="SetTargetADC"/>
Target ADC: 0		
Current ADC: 7064		

Type the target ADC value in the number box and click “SetTargetADC” button to set TargetADC value of device. The device would automatically modify the voltage to maintain CurrentADC to match TargetADC.

5. Set Piezo VOA RDAC (Change the gain of Feedback control)

RDAC1	<input type="text" value="1"/>	<input type="button" value="SetRDAC1"/>
RDAC2	<input type="text" value="1"/>	<input type="button" value="SetRDAC2"/>
Current RDAC:		

Set RDAC1 and RDAC2 value in number box and click “SetRDAC1” and “SetRDAC2” buttons to set the RDAC value. RDACx works as the gain of Feedback control. The bigger the value of RDAC, the attenuation range of VOA would be larger. RDAC1 and RDAC2 can be set a value between 1 and 1023.

For example,

RDAC1=5, RDAC2=1, the attenuation range of VOA is -1 ~ -20 dB.

RDAC1=15, RDAC2=1, the attenuation range of VOA is -20 ~ -40 dB.

The attenuation range would be different for different devices.

If you plan to manually set RDAC for your own implementation, always set RDAC1 first.

6. Manage Table in Flash

- 1) Click “ReadFromFlash” button. A “table.csv” would be created or overwritten.

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- 2) Click "CalibrationTable" button. A window would show as below.

The screenshot shows the 'Calibration Table Generator' window for Channel CH1. It includes fields for MAX_DB (0), RDAC (1), and two columns of 10 ADC and DB values each, all set to 0. Below the table, there are sections for CH2, CH3, and CH4, each preceded by a right-pointing arrow. At the bottom are 'ReadTable' and 'Generate' buttons.

The screenshot shows the 'Calibration Table Generator' window for Channel CH1 after data has been entered. The MAX_DB field is set to 100, and the RDAC field is set to 5. The data table now contains specific values for each ADC and DB pair, such as ADC0: 12442, DB0: 100, and so on for other channels.

- 3) Click "ReadTable" button. All the data from the table would be filled in the window. →

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- 4) Then the window would ready for checking or modifying.
- 5) If any changes are made, click "Generate" button. The "table.csv" would be created or overwritten.
- 6) Click "DownloadTable" button on the main window. The new table would be downloaded into the flash.

Control via UART command (in HEX):

The baud rate setting is 115200-N-8-1.

Basic:

1. Set DB num:
0x01 0x12 <DB higher byte> <DB lower byte>
Return: None
Example: 0x01 0x12 0x03 0xE8 -> set device to -10.00 DB
2. Check Current DB num:
0x01 0x1A 0x00 0x00
Return <Current DB higher byte> <Current DB Lower byte>
Example: 0x01 0x1A 0x00 0x00 RTN: 0x03 0xE8 -> The current DB is set to -10.00 DB
3. Identify Device:
Explain: This command can be used to check whether the correct COM port is used.
0x01 0x02 0x00 0x00
Return 0x41 0x30
4. Check Piezo VOA Board Version:
0x01 0x03 0x00 0x00
Return 0x03 0x00
Explain: If return 0x03 0x00, this board is version 3.0. Otherwise, some functions in this manual may not apply to the board.

Advanced:

1. Set DAC value (VOA voltage):
Explain: This command directly controls the voltage applied to the VOA. This command is for testing.
0x01 0x13 <DAC higher byte> <DAC lower byte> (DAC is a value between 0-4095)
Return <DAC higher byte> <DAC lower byte>
2. Read current VOA voltage:
0x01 0x14 <DAC higher byte> <DAC lower byte>
Return <DAC higher byte> <DAC lower byte>
3. Set Target ADC value:
0x01 0x16 <ADC higher byte> <ADC lower byte>
Return <ADC higher byte> <ADC lower byte>
4. Read ADC status:
Explain: Read current ADC value and target ADC value.
0x01 0x15 0x00 0x00
Return <Current ADC higher byte> <Current ADC lower byte> <Target ADC higher byte> <Target ADC lower byte>

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5. Set RDAC1 value:
0x01 0x17 <RDAC1 higher byte> <RDAC1 lower byte>
Return <RDAC1 higher byte> <RDAC1 lower byte>
6. Set RDAC2 value:
0x01 0x18 <RDAC2 higher byte> <RDAC2 lower byte>
Return <RDAC2 higher byte> <RDAC2 lower byte>
7. Read RDACs value:
0x01 0x19 0x00 0x00
Return <RDAC1 higher byte> <RDAC1 lower byte> <RDAC2 higher byte> <RDAC2 lower byte>
8. Read Flash address:
Explain: This command can be used to read the value of address in device flash.
0x01 0x1C <address high byte> <address low byte>
Return <address byte>

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Appendix I. Full Table in Flash

Table (page 1/3):

Address	Hex	Description
0	0x000	If device need calibration. 0: Not calibrated 1: Already calibrated
1	0x001	0xFF
2	0x002	0xFF
3	0x003	0xFF
4	0x004	Channel 1 Max DB value – high byte
5	0x005	Channel 1 Max DB value – low byte
6	0x006	Channel 1 RDAC1 value – high byte
7	0x007	Channel 1 RDAC1 value – low byte
8	0x008	Channel 1 RDAC2 value – high byte
9	0x009	Channel 1 RDAC2 value – low byte
10	0x00A	Channel 1 ADC Table[0] – high byte
11	0x00B	Channel 1 ADC Table[0] – low byte
12	0x00C	Channel 1 ADC Table[1] – high byte
13	0x00D	Channel 1 ADC Table[1] – low byte
14	0x00E	Channel 1 ADC Table[2] – high byte
15	0x00F	Channel 1 ADC Table[2] – low byte
16	0x010	Channel 1 ADC Table[3] – high byte
17	0x011	Channel 1 ADC Table[3] – low byte
18	0x012	Channel 1 ADC Table[4] – high byte
19	0x013	Channel 1 ADC Table[4] – low byte
20	0x014	Channel 1 ADC Table[5] – high byte
21	0x015	Channel 1 ADC Table[5] – low byte
22	0x016	Channel 1 ADC Table[6] – high byte
23	0x017	Channel 1 ADC Table[6] – low byte
24	0x018	Channel 1 ADC Table[7] – high byte
25	0x019	Channel 1 ADC Table[7] – low byte
26	0x01A	Channel 1 ADC Table[8] – high byte
27	0x01B	Channel 1 ADC Table[8] – low byte
28	0x01C	Channel 1 ADC Table[9] – high byte
29	0x01D	Channel 1 ADC Table[9] – low byte
30	0x01E	Channel 1 DB Table[0] – high byte
31	0x01F	Channel 1 DB Table[0] – low byte
32	0x020	Channel 1 DB Table[1] – high byte
33	0x021	Channel 1 DB Table[1] – low byte
34	0x022	Channel 1 DB Table[2] – high byte
35	0x023	Channel 1 DB Table[2] – low byte
36	0x024	Channel 1 DB Table[3] – high byte
37	0x025	Channel 1 DB Table[3] – low byte
38	0x026	Channel 1 DB Table[4] – high byte
39	0x027	Channel 1 DB Table[4] – low byte
40	0x028	Channel 1 DB Table[5] – high byte

Address	Hex	Description
41	0x029	Channel 1 DB Table[5] – low byte
42	0x02A	Channel 1 DB Table[6] – high byte
43	0x02B	Channel 1 DB Table[6] – low byte
44	0x02C	Channel 1 DB Table[7] – high byte
45	0x02D	Channel 1 DB Table[7] – low byte
46	0x02E	Channel 1 DB Table[8] – high byte
47	0x02F	Channel 1 DB Table[8] – low byte
48	0x030	Channel 1 DB Table[9] – high byte
49	0x031	Channel 1 DB Table[9] – low byte
50	0x032	0xFF
51	0x033	0xFF
52	0x034	Channel 2 Max DB value – high byte
53	0x035	Channel 2 Max DB value – low byte
54	0x036	Channel 2 RDAC1 value – high byte
55	0x037	Channel 2 RDAC1 value – high byte
56	0x038	Channel 2 RDAC2 value – low byte
57	0x039	Channel 2 RDAC2 value – high byte
58	0x03A	Channel 2 ADC Table[0] – low byte
59	0x03B	Channel 2 ADC Table[0] – low byte
60	0x03C	Channel 2 ADC Table[1] – high byte
61	0x03D	Channel 2 ADC Table[1] – low byte
62	0x03E	Channel 2 ADC Table[2] – high byte
63	0x03F	Channel 2 ADC Table[2] – low byte
64	0x040	Channel 2 ADC Table[3] – high byte
65	0x041	Channel 2 ADC Table[3] – low byte
66	0x042	Channel 2 ADC Table[4] – high byte
67	0x043	Channel 2 ADC Table[4] – low byte
68	0x044	Channel 2 ADC Table[5] – high byte
69	0x045	Channel 2 ADC Table[5] – low byte
70	0x046	Channel 2 ADC Table[6] – high byte
71	0x047	Channel 2 ADC Table[6] – low byte
72	0x048	Channel 2 ADC Table[7] – high byte
73	0x049	Channel 2 ADC Table[7] – low byte
74	0x04A	Channel 2 ADC Table[8] – high byte
75	0x04B	Channel 2 ADC Table[8] – low byte
76	0x04C	Channel 2 ADC Table[9] – high byte
77	0x04D	Channel 2 ADC Table[9] – low byte
78	0x04E	Channel 2 DB Table[0] – high byte
79	0x04F	Channel 2 DB Table[0] – low byte
80	0x050	Channel 2 DB Table[1] – high byte
81	0x051	Channel 2 DB Table[1] – low byte
82	0x052	Channel 2 DB Table[2] – high byte
83	0x053	Channel 2 DB Table[2] – low byte
84	0x054	Channel 2 DB Table[3] – high byte
85	0x055	Channel 2 DB Table[3] – low byte
86	0x056	Channel 2 DB Table[4] – high byte

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Appendix I. Full Table in Flash

Table (page 2/3):

Address	Hex	Description
87	0x057	Channel 2 DB Table[4] – low byte
88	0x058	Channel 2 DB Table[5] – high byte
89	0x059	Channel 2 DB Table[5] – low byte
90	0x05A	Channel 2 DB Table[6] – high byte
91	0x05B	Channel 2 DB Table[6] – low byte
92	0x05C	Channel 2 DB Table[7] – high byte
93	0x05D	Channel 2 DB Table[7] – low byte
94	0x05E	Channel 2 DB Table[8] – high byte
95	0x05F	Channel 2 DB Table[8] – low byte
96	0x060	Channel 2 DB Table[9] – high byte
97	0x061	Channel 2 DB Table[9] – low byte
98	0x062	0xFF
99	0x063	0xFF
100	0x064	Channel 3 Max DB value – high value
101	0x065	Channel 3 Max DB value – low value
102	0x066	Channel 3 RDAC1 value – high byte
103	0x067	Channel 3 RDAC1 value – low byte
104	0x068	Channel 3 RDAC2 value – high byte
105	0x069	Channel 3 RDAC2 value – low byte
106	0x06A	Channel 3 ADC Table[0] – high byte
107	0x06B	Channel 3 ADC Table[0] – low byte
108	0x06C	Channel 3 ADC Table[1] – high byte
109	0x06D	Channel 3 ADC Table[1] – low byte
110	0x06E	Channel 3 ADC Table[2] – high byte
111	0x06F	Channel 3 ADC Table[2] – low byte
112	0x070	Channel 3 ADC Table[3] – high byte
113	0x071	Channel 3 ADC Table[3] – low byte
114	0x072	Channel 3 ADC Table[4] – high byte
115	0x073	Channel 3 ADC Table[4] – low byte
116	0x074	Channel 3 ADC Table[5] – high byte
117	0x075	Channel 3 ADC Table[5] – low byte
118	0x076	Channel 3 ADC Table[6] – high byte
119	0x077	Channel 3 ADC Table[6] – low byte
120	0x078	Channel 3 ADC Table[7] – high byte
121	0x079	Channel 3 ADC Table[7] – low byte
122	0x07A	Channel 3 ADC Table[8] – high byte
123	0x07B	Channel 3 ADC Table[8] – low byte
124	0x07C	Channel 3 ADC Table[9] – high byte
125	0x07D	Channel 3 ADC Table[9] – low byte
126	0x07E	Channel 3 DB Table[0] – high byte
127	0x07F	Channel 3 DB Table[0] – low byte
128	0x080	Channel 3 DB Table[1] – high byte
129	0x081	Channel 3 DB Table[1] – low byte
130	0x082	Channel 3 DB Table[2] – high byte
131	0x083	Channel 3 DB Table[2] – low byte
132	0x084	Channel 3 DB Table[3] – high byte

Address	Hex	Description
133	0x085	Channel 3 DB Table[3] – low byte
134	0x086	Channel 3 DB Table[4] – high byte
135	0x087	Channel 3 DB Table[4] – low byte
136	0x088	Channel 3 DB Table[5] – high byte
137	0x089	Channel 3 DB Table[5] – low byte
138	0x08A	Channel 3 DB Table[6] – high byte
139	0x08B	Channel 3 DB Table[6] – low byte
140	0x08C	Channel 3 DB Table[7] – high byte
141	0x08D	Channel 3 DB Table[7] – low byte
142	0x08E	Channel 3 DB Table[8] – high byte
143	0x08F	Channel 3 DB Table[8] – low byte
144	0x090	Channel 3 DB Table[9] – high byte
145	0x091	Channel 3 DB Table[9] – low byte
146	0x092	0xFF
147	0x093	0xFF
148	0x094	Channel 4 Max DB value – high value
149	0x095	Channel 4 Max DB value – low value
150	0x096	Channel 4 RDAC1 value – high byte
151	0x097	Channel 4 RDAC1 value – low byte
152	0x098	Channel 4 RDAC2 value – high byte
153	0x099	Channel 4 RDAC2 value – low byte
154	0x09A	Channel 4 ADC Table[0] – high byte
155	0x09B	Channel 4 ADC Table[0] – low byte
156	0x09C	Channel 4 ADC Table[1] – high byte
157	0x09D	Channel 4 ADC Table[1] – low byte
158	0x09E	Channel 4 ADC Table[2] – high byte
159	0x09F	Channel 4 ADC Table[2] – low byte
160	0x0A0	Channel 4 ADC Table[3] – high byte
161	0x0A1	Channel 4 ADC Table[3] – low byte
162	0x0A2	Channel 4 ADC Table[4] – high byte
163	0x0A3	Channel 4 ADC Table[4] – low byte
164	0x0A4	Channel 4 ADC Table[5] – high byte
165	0x0A5	Channel 4 ADC Table[5] – low byte
166	0x0A6	Channel 4 ADC Table[6] – high byte
167	0x0A7	Channel 4 ADC Table[6] – low byte
168	0x0A8	Channel 4 ADC Table[7] – high byte
169	0x0A9	Channel 4 ADC Table[7] – low byte
170	0x0AA	Channel 4 ADC Table[8] – high byte
171	0x0AB	Channel 4 ADC Table[8] – low byte
172	0x0AC	Channel 4 ADC Table[9] – high byte
173	0x0AD	Channel 4 ADC Table[9] – low byte
174	0x0AE	Channel 4 DB Table[0] – high byte
175	0x0AF	Channel 4 DB Table[0] – low byte
176	0x0B0	Channel 4 DB Table[1] – high byte
177	0x0B1	Channel 4 DB Table[1] – low byte
178	0x0B2	Channel 4 DB Table[2] – high byte

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Appendix I. Full Table in Flash

Table (page 3/3):

Address	Hex	Description
179	0x0B3	Channel 4 DB Table[2] – low byte
180	0x0B4	Channel 4 DB Table[3] – high byte
181	0x0B5	Channel 4 DB Table[3] – low byte
182	0x0B6	Channel 4 DB Table[4] – high byte
183	0x0B7	Channel 4 DB Table[4] – low byte
184	0x0B8	Channel 4 DB Table[5] – high byte
185	0x0B9	Channel 4 DB Table[5] – low byte
186	0x0BA	Channel 4 DB Table[6] – high byte
187	0x0BB	Channel 4 DB Table[6] – low byte
188	0x0BC	Channel 4 DB Table[7] – high byte
189	0x0BD	Channel 4 DB Table[7] – low byte
190	0x0BE	Channel 4 DB Table[8] – high byte
191	0x0BF	Channel 4 DB Table[8] – low byte
192	0x0C0	Channel 4 DB Table[9] – high byte
193	0x0C1	Channel 4 DB Table[9] – low byte
194	0x0C2	0xFF
195	0x0C3	0xFF
196	0x0C4	DAC Table[0] – high byte
197	0x0C5	DAC Table[0] – low byte
198	0x0C6	DAC Table[1] – high byte
199	0x0C7	DAC Table[1] – low byte
200	0x0C8	DAC Table[2] – high byte
201	0x0C9	DAC Table[2] – low byte
202	0x0CA	DAC Table[3] – high byte
203	0x0CB	DAC Table[3] – low byte
204	0x0CC	DAC Table[4] – high byte
205	0x0CD	DAC Table[4] – low byte
206	0x0CE	DAC Table[5] – high byte
207	0x0CF	DAC Table[5] – low byte
208	0x0D0	DAC Table[6] – high byte
209	0x0D1	DAC Table[6] – low byte
210	0x0D2	DAC Table[7] – high byte
211	0x0D3	DAC Table[7] – low byte
212	0x0D4	DAC Table[8] – high byte
213	0x0D5	DAC Table[8] – low byte
214	0x0D6	DAC Table[9] – high byte
215	0x0D7	DAC Table[9] – low byte
216	0x0D8	DB Table[0] – high byte
217	0x0D9	DB Table[0] – low byte
218	0x0DA	DB Table[1] – high byte
219	0x0DB	DB Table[1] – low byte
220	0x0DC	DB Table[2] – high byte
221	0x0DD	DB Table[2] – low byte
222	0x0DE	DB Table[3] – high byte
223	0x0DF	DB Table[3] – low byte
224	0x0EO	DB Table[4] – high byte

Address	Hex	Description
225	0x0E1	DB Table[4] – low byte
226	0x0E2	DB Table[5] – high byte
227	0x0E3	DB Table[5] – low byte
228	0x0E4	DB Table[6] – high byte
229	0x0E5	DB Table[6] – low byte
230	0x0E6	DB Table[7] – high byte
231	0x0E7	DB Table[7] – low byte
232	0x0E8	DB Table[8] – high byte
233	0x0E9	DB Table[8] – low byte
234	0x0EA	DB Table[9] – high byte
235	0x0EB	DB Table[9] – low byte
236	0x0EC	0xFF
237	0x0ED	0xFF
238	0x0EE	0xFF
239	0x0EF	0xFF
240	0x0F0	0xFF
241	0x0F1	0xFF
242	0x0F2	0xFF
243	0x0F3	0xFF
244	0x0F4	0xFF
245	0x0F5	0xFF
246	0x0F6	0xFF
247	0x0F7	0xFF
248	0x0F8	0xFF
249	0x0F9	0xFF
250	0x0FA	0xFF
251	0x0FB	0xFF
252	0x0FC	0xFF
253	0x0FD	0xFF
254	0x0FE	0xFF
255	0x0FF	0xFF